Highly Ultraviolet Light Sensitive and Highly Reliable Photodiode with Atomically Flat Si Surface

Rihito Kuroda, Taiki Nakazawa, Katsuhiko Hanzawa and Shigetoshi Sugawa
Graduate School of Engineering, Tohoku University
6-6-11-811, Aza-Aoba, Aramaki, Aoba-ku, Sendai, Miyagi, Japan 980-8579
TEL: +81-22-795-4833, FAX: +81-22-795-4834, Email address: kuroda@fff.niche.tohoku.ac.jp

ABSTRACT

Highly UV-light sensitive and highly reliable FSI-photodiode is demonstrated in this work. Using the atomically flat Si surface to uniformly form the thin surface drift layer, a photodiode exhibiting the almost 100% internal Q.E. to UV-Visible-Near IR light and a high stability to UV-light is obtained. The developed photodiode process is compatible to the current manufacturing processes for FSI-photodiodes, arrayed sensors and image sensors.

INTRODUCTION AND PROPOSED PHOTODIODE CONCEPT

Ultraviolet light (UV-light) sensing and imaging are widely required in the fields of biological phenomena analysis, space application, environmental assessment and various types of spectrophotometric analyses [1-4]. Highly UV-light sensitive and highly reliable photodiodes and arrayed sensors as well as, a stable and cost effective manufacturing process suitable for mass production are therefore strongly desired.

Fig. 1 shows the depth from Si surface where the amount of incident light decreases to 90 % and 37 % due to the absorption as a function of the wavelength, calculated by the absorption coefficient in Si. Due to its high absorption coefficient, most of the UV-light in Si is absorbed within the top few atomic layers. Because of this, conventional buried photodiodes used in the current image sensors do not have any UV-light sensitivity. To increase the UV-light sensitivity, the atomic scale control of the surface dopant profile to form the surface drift layer is fundamentally required. However, the conventional fabrication process induces an unsuitable large roughness to Si surface, as displayed in Fig.2, where the AFM images are shown for an atomically flat Si(100) surface and a typical Si(100) surface after the RCA cleaning with relatively low ammonia concent-ration in ammonia-peroxide solution [5]. As compared to the atomically flat surface, the conventional surface has much large roughness with peak to valley (P-V) of larger than 1 nm.

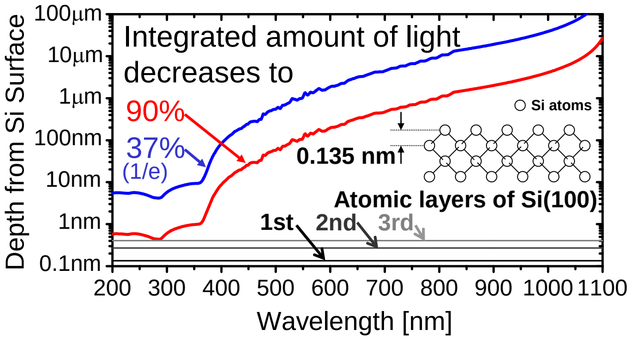
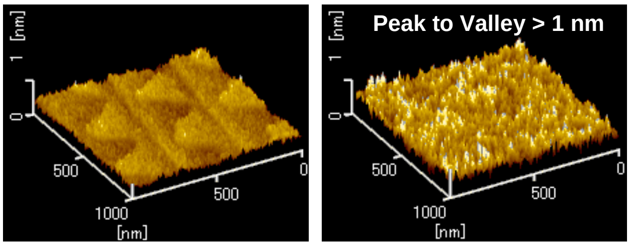


Fig. 1 Depth from Si surface where the amount of incident light decreases to 90% and 37% due to the absorption as a function of wavelength.



(a) (b)

Fig. 2 AFM images of (a) an atomically flat Si(100) surface and (b) a typical Si(100) surface after RCA cleaning.

In addition, due to the high photon energy of UV-light, stability to light exposure is indispensable for the long time use of UV-light sensors [6-7]. Recently, an UV-light sensitive BSI-CCD using highly doped Si molecular beam epitaxy on the back surface was reported [8-9].

In this work, we demonstrate a highly UV-light sensitive and highly reliable FSI-photodiode using the atomically flat Si surface, compatible to the current photodiode and image sensor fabrication processes. Using the technologies to atomically flatten the Si surface and preserve the flatness throughout the fabrication [10-12], buried photodiodes were fabricated with uniformly formed few nanometer-thick surface high concentration layers. This surface high concentration layer induces an electrical field that drifts the photo-generated carriers to the buried photodiode without the recombination at the interface states, leading to the high sensitivity characteristic to UV-Visible-Near IR light.

EXPERIMENTAL SETUP

The atomically flat surface is obtained due to the migration of Si atoms by annealing an off-angle-controlled Si wafer in pure Ar ambient at 850°C or a higher temperature [10, 12]. The modified process technologies of wafer surface cleaning and insulator film formation were employed as summarized in Fig.3 [10-11]. By introducing all of these technologies, the atomically flat SiO_2/Si interface is able to be formed. Fig.4 shows the AFM images and cross section profiles of the atomically flat Si surfaces. Surfaces are composed of atomic terraces and atomic steps with the height equals to one atomic layer of Si(100): 0.135nm. The surface step morphology can be controlled by the wafer off angle and direction. As illustrated in Fig.5, it is considered that with the conventional flatness, the thin surface drift layer is not uniformly formed and many spots appear where the carrier recombination and generation occurs with very short relaxation time constants due to the interface states, On the contrary, with the atomically flat surface, the thin surface drift layer is uniformly formed and these sensitivity loss and dark current generation spots do not appear.

The n^+pn buried photodiodes were fabricated on Cz-n Si(100) wafers (dopant concentration: $1x10^{15}cm^{-3}$) with the atomically flat and the conventional flat surfaces.

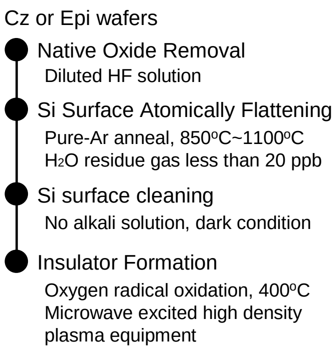
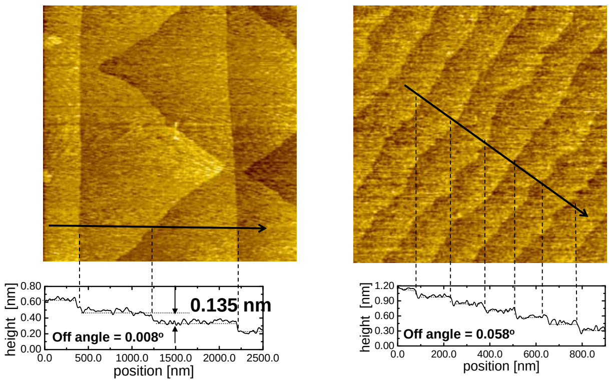
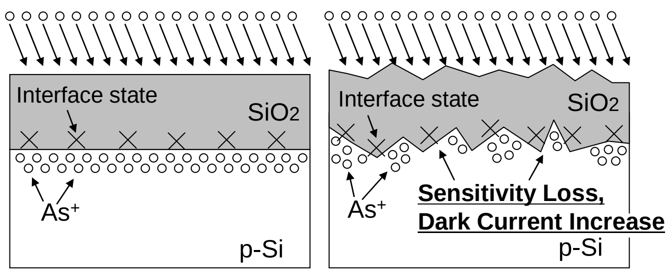


Fig. 3 Process technologies to form the atomically flat Si surface and to preserve the flatness during the fabrication.



(a) (b)

Fig. 4 (a) 3x3 μm^2 and (b) 1x1 μm^2 AFM images and cross section profiles of Si(100) surfaces after the flattening process.



(a) (b)

Fig. 5 Schematic images of the cross section of surface thin n^+ layer formed on (a) the atomically flat and (b) the conventional flat Si surfaces, respectively.

Figs.6 and 7 show the fabrication flow and structure of the photodiodes. The buried p-Si layer has dopant concentration of $2x10^{17}$ cm^{-3} and thickness of 250 nm, while the surface n^+ layer thickness is varied from 0 to 30 nm for different wafers.

In this work, the surface drift layer was formed by the As^+ implantation. As^+ implantation is considered to be advantageous because of its heavy mass, high solubility and small diffusion constant in Si and tendency to segregate at the Si/SiO_2 interface during the activation anneal. The As^+ implantation conditions were varied for wafers to examine the impact of the profile and the thickness of surface n^+ layer to the characteristics of fabricated photodiodes. Typical depth profiles of As measured by secondary ion mass spectroscopy (SIMS) are shown in Fig.8. Table 1 summarizes the fabrication conditions and the extracted surface n^+ layer thicknesses.

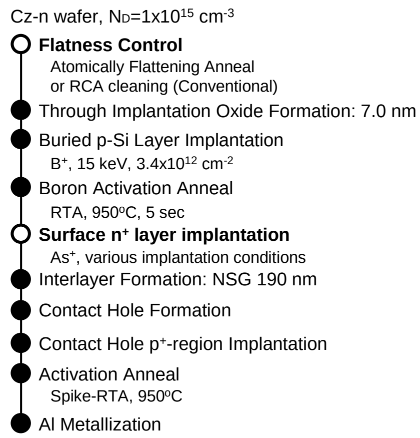
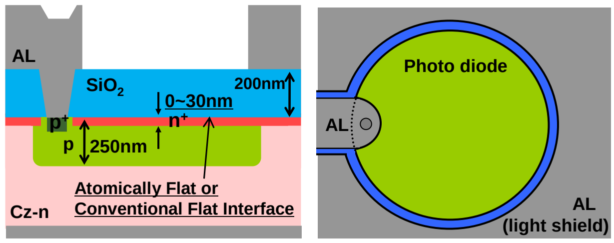


Fig. 6. Photodiode fabrication flow.



(a) (b)

Fig. 7 Schematic images of the fabricatd n^+pn photodiodes, (a) the cross sectional veiw and (b) the birds-eye view.

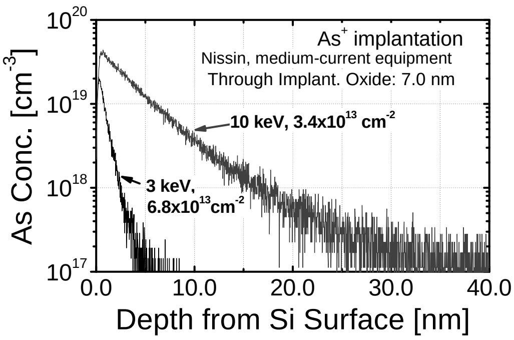


Fig. 8 Profiles of As from the Si surface measured by SIMS for wafer numbers 2 and 4 in table 1.

Table 1
Fabricated device condtions

No.	Flatness	As^+ implantation		Surface n^+ layer thickness [nm]
		Energy [keV]	Dose [cm^{-2}]	
1	Conventional Flat	-	0	0
2	Atomically Flat	3	$6.8x10^{13}$	3.5
3	Conventional Flat	3	$6.8x10^{13}$	3.5
4	Atomically Flat	10	$3.4x10^{13}$	30.0

The dark current, photo-current and quantum efficiency (Q.E.) as well as, Q.E. and dark current stability to UV-light were evaluated using the on-wafer characterization system shown in Fig.9. The measured range of wavelength is 200-1000 nm. Fig.10 shows the characteristic of the UV-light source used for the UV-light exposure stress. The super high pressure mercury discharge lump was employed. The typical UV-light intensities are 2.0, 4.4, 8.8 and 17.6 mW/cm^2 for λ = 254, 303, 313 and 365 nm, respectively. The stability to UV-light was evaluated up to the exposure time of 1000 min while the photodiodes were either reverse biased at -2.0 V or floating during the exposure. The total amount of the light exposure after 1000 min are $1.2x10^2$, $2.6x10^2$, $5.3x10^2$ and $1.1x10^3$ J/cm^2 for λ = 254, 303, 313 and 365 nm, respectively.

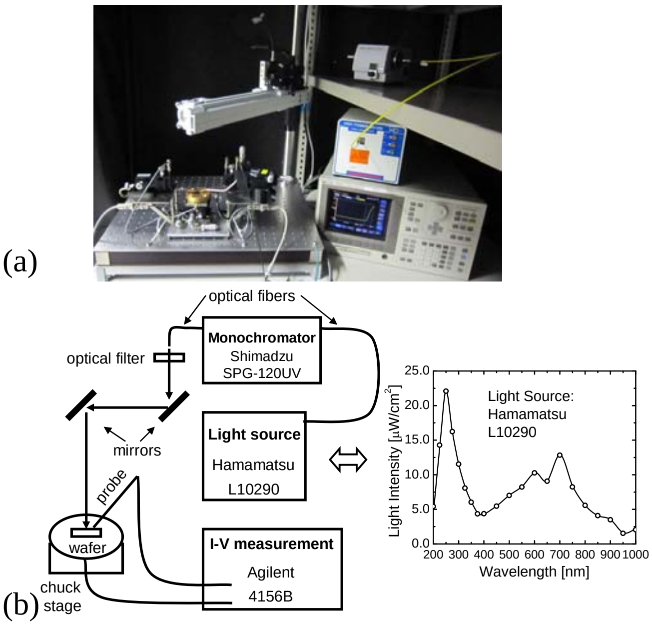


Fig. 9 (a) picture and (b) schematic images of the on-wafer dark current and photo-current measurement system.

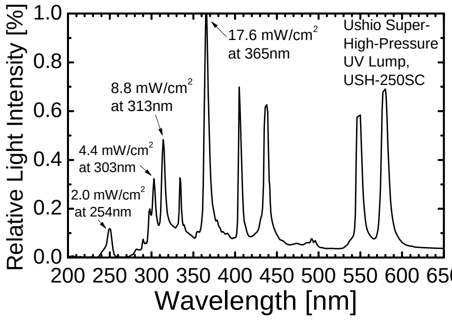


Fig. 10 Characteristic of the UV-light source used for the UV-light exposure stress.

RESULTS AND DISCUSSION

Fig.11 shows the measured pn junction J-V characteristics of the fabricated photodiodes with and without light. The absolute value of the dark current is relatively high due to the unoptimized process of the pn junction formation. For the atomically flat device with 10keV As^+ implantation, the reverse current density is smaller than without n^+ layer. Higher current density for devices with 3keV As^+ implantation indicates excess interface states creation during the through oxide As^+ implantation. Fig.12 shows the measured external and internal Q.E. as a function of the wavelength. The 100% internal Q.E. is calculated by the n and k values of 200nm-thick SiO_2 film formed above the photodiodes. With the atomically flat Si surface, very high Q.E. is obtained for 200-1000nm, while with the conventional flatness or without surface n^+ layer, Q.E. in UV-light range is very low. It is considered that the slight decrease of the Q.E. for wavelength longer than 400 nm is due to the shallow p-Si layer (250nm). This will be overcome by the optimization of p-Si layer thickness. Fig.13(a-b) shows the dark current and external Q.E. at 250 nm as a function of the surface n^+ layer thickness. The impact of the atomically flatness is clearly confirmed in the average values and the variations when the n^+ layer thickness is 3.5 nm, indicating that the atomically flat Si surface can enlarge the process margin for the formation of suitable surface drift layer.

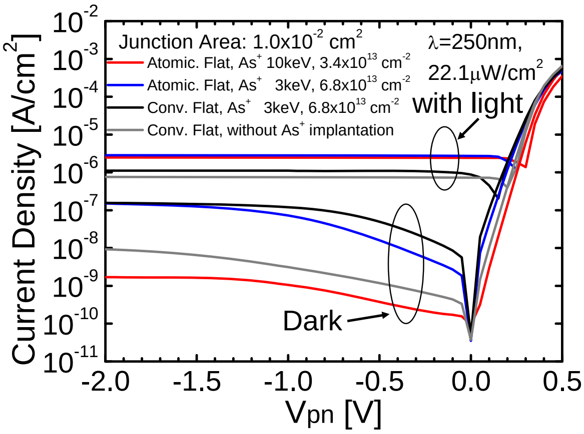


Fig. 11 Measured pn junction J-V characteristics of the fabricated photodiodes with and without light.

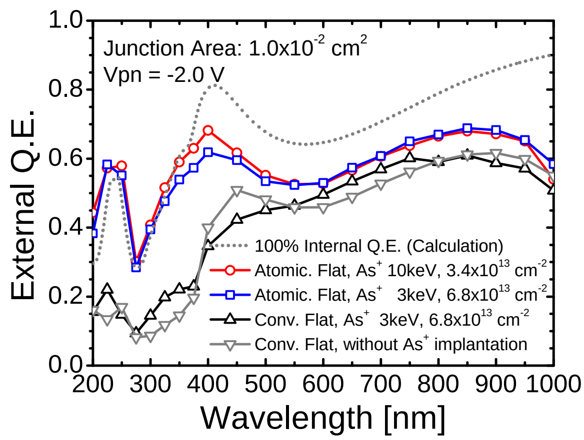


Fig. 12 Measured external Q.E. as a function of the wavelength.

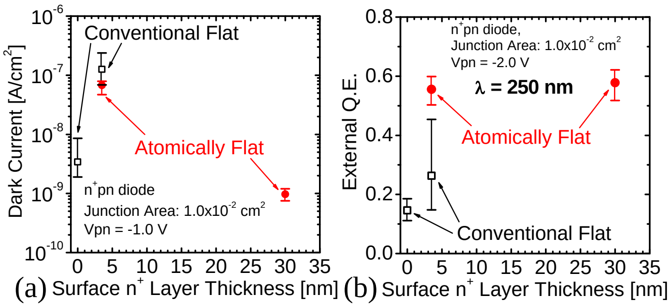


Fig. 13 (a) dark current and (b) External Q.E. at 250 nm as a function of the surface n^+ layer thickness. 5 samples were evaluated for each condition.

Figs.14 and 15 show the external Q.E. as a function of the wavelength measured at various UV-light exposure time and the internal Q.E. at 250 nm as a function of the UV-light exposure time up to 1000 min, respectively. The photodiodes were either reverse biased at -2.0 V or floating during the UV-light exposure. The fabrication conditions are shown in the figures. For the atomically flat device with As^+ implantation condition of 10keV, $3.4x10^{13}$ cm^{-2}, almost no degradation occurred for the UV-Visible-NearIR light, and the almost 100 % internal Q.E. is maintained throughout the UV-light exposure time. With As^+ implantation condition of 3keV, $6.8x10^{13}$ cm^{-2}, the atomically flat device initially shows the almost 100 % internal Q.E., however a large degradation of Q.E. to UV-light occurred after 10 min. For the conventional flat device, Q.E. to UV-light is low at the all measured times, and a slight degradation is observed in the UV-light range. For each device, the behaviors of the Q.E. to the UV-light exposure are almost the same between the two bias conditions during the UV-light exposure.

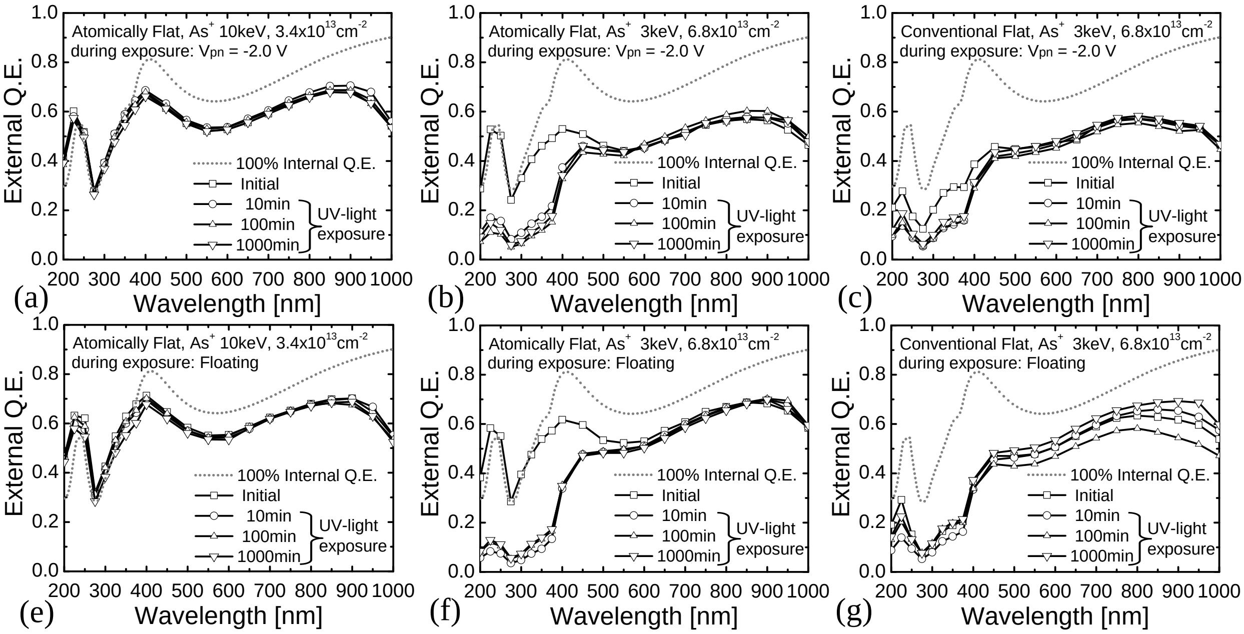


Fig. 14 External Q.E. measured as a function of the wavelength at various UV-light exposure time. The fabrication conditions and the pn-junction bias conditions during UV-light exposure are shown in the figures. The photodiode area is 1.0x10^{-2} cm^2.

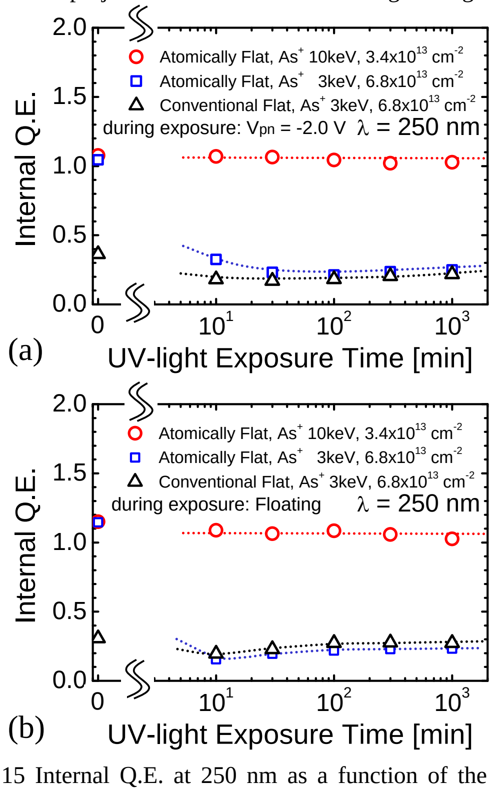


Fig. 15 Internal Q.E. at 250 nm as a function of the UV-light exposure time, while the photodiodes were (a) reverse biased at -2.0 V and (b) floating. The photodiode area is 1.0x10^{-2} cm^2.

CONCLUSION

By introducing the atomically flat Si surface to uniformly form the thin surface drift layer, a photodiode exhibiting the almost 100% internal Q.E. to UV-Visible-NearIR light and a high stability to UV-light is demonstrated. The atomically flatness was found to be effective to enlarge the process margin to form the suitable surface drift layer. The developed FSI-photodiode process is compatible to the current photodiode manufacturing, and it is a promising technology for the development of highly UV-light sensitive and highly reliable Si photodiodes, arrayed sensors and image sensors.

ACKNOWLEDGEMENT

Authors would like to acknowledge Y. Kondo and K. Takubo of Shimadzu Corp. for their support on photodiode evaluation.

REFERENCES

[1] T. Haraguchi D-Q. Ding, A. Yamamoto, T. Kaneda, T. Koujin and Y. Hiraoka, “Multiple-color Fluorescence Imaging of Chromosomes and Microtubules in Living Cells,” Cell Structure and Function, Vol.24, pp.291-298, 1999.

[2] P. E. Malinowski J. Y. Duboz, P. D. Moor, J. John, K. Minoglou, P. Srivastava, Y. Creten, T. Torfs, J. Putzeys, F. Semond et al., “10 µm Pixel-to-Pixel Pitch Hybrid Backside Illuminated AlGaN-on-Si Imagers for Solar Blind EUV Radiation Detection,” IEDM Tech. Dig., pp.348-351, 2010.

[3] Y. Goldberg, “Semiconductor near-ultraviolet photoelectronics,” Semicond. Sci. Technol. Vol.14, pp.R41-60, 1999.

[4] B. E. Lendi and V. R. Meyer, “The UV Detector for HPLC -An Ongoing Success Story-,” Liquid Chromatography - Gas Chromatography (LC-GC) Europe, Vol.18, pp.156-163, 2005.

[5] T. Ohmi, M. Miyashita, M. Itano, T. Imaoki and I. Kawanabe, “Dependence of Thin-Oxide Films Quality on Surface Microroughness,” IEEE T-ED., Vol. 39, pp. 537-545, 1992.

[6] F. M. Li, N. O and A. Nathan, “Degradation Behavior and Damage Mechanisms of CCD Image Sensor With Deep-UV Laser Radiation,” IEEE T-ED, Vol. 51, pp.2229-2236, 2004.

[7] T. Watanabe, J-H. Park, S. Aoyama, K. Isobe and S. Kawahito, “Effects of Negative Bias Operation and Optical Stress on Dark Current,” IISW, Session 05-p8, 2009.

[8] S. Nikzad M. E. Hoenk, J. Blacksberg, T. J. Jones and T. J. Cunningham, S. E. Holland, W. Kolbe and C. Bebek, “High Performance Large Format UV/optical/near IR Detector Arrays,” IISW, pp.181-183, 2007.

[9] J. Blacksberg, S. Nikzad, M. E. Hoenk, S. E. Holland and W. F. Kolbe, “Near-100% Quantum Efficiency of Delta Doped Large-Format UV-NIR Silicon Imagers,” IEEE T-ED, Vol.55, pp.3402-3406, 2008.

[10] R. Kuroda, T. Suwa, A. Teramoto, R. Hasebe, S. Sugawa and T. Ohmi, “Atomically Flat Silicon Surface and Silicon/ Insulator Interface Formation Technologies for (100) Surface Orientation Large-Diameter Wafers Introducing High Performance and Low-Noise Metal-Insulator-Silicon FETs,” IEEE T-ED, Vol.56, pp.291-298, 2009.

[11] R. Kuroda, A. Teramoto, Y. Nakao, T. Suwa, M. Konda, R. Hasebe, X. Li, T. Isogai, H. Tanaka, S. Sugawa and T. Ohmi, “Complementary Metal–Oxide–Silicon Field-Effect-Transistors Featuring Atomically Flat Gate Insulator Film/Silicon Interface,” Jpn. J. Appl. Phys., Vol. 48, pp.04C048-1-6, 2009.

[12] X. Li, A. Teramoto, T. Suwa, R. Kuroda, S. Sugawa and T. Ohmi, “Atomically Flattening Technology at 850°C for Si(100) Surface,” ECS Trans. Vol.28, pp.299-309, 2010.